ANALYSIS OF A 1.5-V 900-MHZ MONOLITHIC CMOS FAST-SWITCHING FREQUENCY SYNTHESIZER FOR WIRELESS APPLICATIONS

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Abstract: A recurrence synthesizer is a standout amongst the most basic building hinders in any remote handset framework. Its configuration is getting increasingly difficult as the interest for low-voltage low-control high-recurrence remote frameworks consistently develops. As the supply voltage is diminished, numerous current configuration strategies are no more appropriate. This book gives the peruser models and outline methods that empower CMOS recurrence synthesizers to work at low supply voltages, at high frequencies with good stage commotion and with low power utilization. Notwithstanding redesigning the peruser on a hefty portion of these strategies top to bottom, this book will likewise present helpful rules and regulated methodology on conduct reenactments of recurrence synthesizers. At last, three effectively exhibited CMOS synthesizer models withdetailed plan thought and depiction will be displayed to outline potential uses of the structures and outline methods portrayed. The book is expected for architects, directors and analysts who are working or intrigued by radio-recurrence incorporated circuit plan for remote applications.

1. Introduction:

A recurrence synthesizer is a standout amongst the most basic building obstructs in any incorporated remote handset framework. Its configuration is getting increasingly difficult as the interest for low-voltage low-control high-recurrence remote frameworks is constantly expanded. In the meantime, CMOS forms have progressed and been appeared to be increasingly appealing because of their potential in accomplishing frameworks with the most astounding joining level and the least cost. Then again, as the supply voltage is brought down, numerous current configuration procedures for incorporated recurrence synthesizers are no more pertinent. Be that as it may, it is still attractive to plan RF recurrence synthesizers at low supply voltages not just due to the gadget unwavering quality because of the innovation scaling additionally in view of the combination and similarity with digital circuits.

There are as of now just a couple books accessible on incorporated RF CMOS recurrence synthesizers. The most far reaching book on incorporated CMOS recurrence synthesizers accessible today is entitled Wireless CMOS Frequency
Synthesizer Design by Craninckx and Steyaert (1998). All the more as of late, another book entitled Multi-GHz Frequency Synthesis and Division by Rateghand Lee was additionally distributed in 2001. While the two books are still very valuable, they concentrate just on cutting edge outline systems of some chose building pieces, including voltage-controlled oscillators, dividers, and synthesizers, with accentuation just on a specific design. There exist numerous new synthesizer models and plan methods that are not secured in point of interest.

System Design

Phase-locked loop synthesizer

There are many methods to synthesize a required frequency from a frequency reference source. The most common methods are direct analog synthesis, direct digital synthesis and phase-locked loop synthesis7, 8. However, most of the frequency synthesizer designs are dominated by phase-locked loop designs because they are simpler, smaller and less power-consuming. The basic block diagram is shown in Fig. 14. The voltage-controlled oscillator outputs a signal of frequency fout. Then the signal fout will be divided by a programmable digital counter. The frequency and phase of the resultant signal is then compared to the frequency and phase of the reference signal fref by a mixer or a frequency-phase detector. The output signal of the mixer or frequency-phase detector is filtered out by a low-pass filter. The signal at the filter output is an error signal which represents the difference of phase and frequency of the reference signal fref and the divided signal fout/N and is used to control the voltage-controlled oscillator such that the signal fout/N equals to fref, or fout equals to N x fref.

Fig. 1 Block diagram of phase-locked loop frequency synthesizer

However, since the closed loop response of the phase-locked loop synthesizer is lowpass, the response of the phase-locked loop synthesizer for any change of the frequency of the output signal is quite slow. The fast change of the output frequency is very important in time-division dualplex and frequency-hopping systems. The change of the output frequency is done by the change of the modulus selection word.

Fractional-N synthesizer

The above-proposed architecture provides a simple solution to increase the frequency switching speed of phase-locked loop frequency synthesizers. There are also many
variations of the basic phase-locked loop frequency synthesizer to increase the performance of the synthesizer. One of the variations is the multi-loop phase-locked loop frequency synthesizer which employs two or more phase-locked loop frequency synthesizers. The most common design is dual-loop phase-locked loop frequency synthesizers. There can be a number of different configurations. One of the frequency synthesizer can generate the reference frequency to the other frequency synthesizer, as shown in Fig. 16a. Or, one of the frequency synthesizer can generate a frequency offset added or subtracted from the other frequency synthesizer, as shown in Fig. b.

Fig. 2 Block diagrams of some dual-loop synthesizer designs

In the original phase-locked loop frequency synthesizer (Integer-N frequency synthesizer), the output frequency \( f_{\text{out}} \) which equals to \( N \times f_{\text{ref}} \), is an integral multiple of the reference frequency \( f_{\text{ref}} \) because the frequency divider can only have integer division ratio. However, by continuously changing the division ratio of the frequency divider, it is possible to have an average division ratio which is a fractional number. For example, if a frequency divider have the division ratio 4 in 50% of time and the division ratio 5 in the other 50% of time. The average division ratio will be 4.5. This is referred to a fractional-N frequency synthesizer.

The fractional-N frequency synthesizer is actually an integer-N frequency synthesizer with a changing division ratio in the frequency divider. Only some additional digital circuits are needed to generate a continuously changing division ratio. This makes the design to be more simple and robust than the multi-loop frequency synthesizer as multiple hardware of the multi-loops, filters and mixers are needed in multi-loop frequency synthesizer. Therefore, this design is based on fractional-N PLL architecture.

Design criteria

One drawback of the fractional-N synthesizer is that quantization noise is
added to the loop because there are only a few division ratios (quantization level) in the frequency divider but they will represent the division ratios in between. In the case of a constant fractional division ratio required, the quantization noise generated is a single frequency tone, as shown in Fig. 3a, in which the frequency depends on the fractional division ratio. In case of a random changing division ratio required, the quantization noise generated has a white noise spectrum as shown in Fig. 3b. To solve the problem, a sigma-delta modulator can be used before the divider 10. For a fractional number input (Fig. 4a), the sigma-delta modulator can redistribute the quantization noise such that the most of the noise is located at higher frequencies (Fig. 4b). The resultant high frequency noise can be filtered out by the low-pass response of the loop (Fig. 4c), and very little noise is left.

Fig. 3 Quantization noise in frequency domain

Fig. 4 Quantization noise in a sigma-delta Fractional-N synthesizer

To design a fractional-N PLL synthesizer, three parameters, including reference frequency, loop bandwidth, number of orders of the sigma-delta modulator, have to be determined. These parameters mainly determine the switching speed, spurs and noise of the loop.

4 Circuit Implementation

Voltage-controlled oscillator

Quaduature LC oscillators

The voltage-controlled oscillator, as shown in Fig. 21, includes two identical differential LC oscillators which are mutually coupled by four coupling transistors to provide
quadrature phase outputs\textsuperscript{11}. The LC oscillator employs two-layer (metal 2 and metal 3) spiral inductors. Each oscillator contains an 8-bit switchable-capacitor-array as the main frequency tuning and two small varactors as the fine frequency tuning.

![Fig. 5 The schematic diagram of the voltage-controlled oscillator with switchable-capacitor-array](image)

The coupled-LC oscillators can be viewed as two LC oscillators put in a four-stage ring oscillators, as shown in Fig. 22. Each stage of the ring oscillator has a phase shift of 90 degrees. Inside this frame of the ring oscillator, the two LC oscillators will have a 90-degree phase difference between their outputs. As the noisy ring oscillator maintains the quadrature phases, the two LC oscillators maintain the purity of frequency. By sharing the current sources, both amplitude and phase matchings of the outputs of the two oscillators are even better maintained\textsuperscript{12}.

![Fig. 6 Another view of coupled LC oscillators](image)

**Conclusion**

In this investigation, the major objective is to realize a world class repeat synthesizer for the strong GSM authority. Remembering the finished objective to handle the distinctive issues went up against, a couple of techniques on the repeat synthesizer structure and the circuits of the building pieces are proposed.

In the repeat synthesizer structure, signals in essential ways are proposed to be set up in capacitance range instead of voltage and current space. In light of this proposed thought, a twofold weighted switchable-capacitance display is used to supplant the progressed to-straightforward converter while two varactors related in parallel supplant the voltage snake. This philosophy gives the upsides of unraveled and couple of basic equipment (e.g. fundamental charge...
pump, no voltage snake, modernized to-straightforward converter and linearization equipment), low supply voltage, low power usage, little chip zone, snappy repeat trading and high resistance of substrate uproar.

Another change considering the capacitance space operation is the circle channel. By using the two methods for the twofold path channel to control two varactors in the voltagecontrolled oscillators, the dependence of the two ways is broken. The low-pass channel way which can't give any tuning degree can be planned to enhance for commotion. Around half of the capacitors can be diminished by this change. Additionally, since no voltage snake is required, the proposed approach minimizes both disturbance and power usage.

As the voltage-controlled oscillator is the most basic building thwart in the repeat synthesizer, some circuit systems are furthermore proposed to improve its execution. A technique by joining the present wellsprings of the coupled-LC oscillators can give an exceptional abundance planning control and update the quadrature stage organizing.

Examination on the design of the LC oscillator for the perfect upheaval execution is furthermore done. Considering this, the framework frameworks are discussed and a sharp thought to diminish the plenitude uproar component is proposed. The proposed thought raises the probability of zero plenitude racket variable in the LC oscillator diagram.

Brushing on the above system and circuit methodology proposed, another diagram of repeat synthesizer is realized. The repeat synthesizer in like manner uses the sigma-delta fragmentary configuration to encourage enhance the shows. The model of this repeat synthesizer has been formed and made to display the proposed techniques and considerations.

An expansive part of the intentional parameters meet the framework points of interest including the repeat range, repeat determination, settling time, circle information exchange limit, supply voltage, power usage and chip domain. Likewise, this repeat synthesizer is the principle reported setup which can work with a 1.5-V supply voltage and have 0.9mm x 1.1mm chip range.

The stage upheaval execution is 1dB lower than the setup regard in light of the way that the shocking low quality segment of the inductor. The prods, which can't be foreseen, are extremely significant in perspective of the mighty arrangement. In any case, as a result of the vigilant choice of the reference repeat, the prods at 25.6MHz won't be a noteworthy issue in the 140 beneficiary structure. As a result of the issue of testing setup, the GMSK change can't be attempted. Simply the FSK change can be attempted.
yet it can at present demonstrate the limit of electronic alteration of the repeat synthesizer

Bibliography


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