A NOVEL WALLACE TREE MULTIPLIER FOR USING FAST ADDERS

G.Ramesh 1*, K.Naga Lakshmi 2*

1. II. M.Tech (VLSI), Dept of ECE, AM Reddy Memorial College of Engineering & Technology, Petlurivaripalem.

ABSTRACT

Designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is Wallace tree multiplier. Wallace Tree CSA structures have been used to sum the partial products in reduced time. In this paper Wallace tree construction is investigated and evaluated. Speed of traditional Wallace tree multiplier can be improve by using compressor techniques. In this paper Wallace tree is constructed by traditional method and with the help of compressor techniques such as 4:2 compressor, 5:2 compressor, 6:2 compressor, 7:2 compressor. Therefore, minimizing the number of half adders used in a multiplier reduction will reduce the complexity

I. INTRODUCTION

The digital signal processing (DSP) is one of the core technologies in multimedia and communication systems. Many application systems based on DSP, especially the recent next-generation optical communication systems, require extremely fast processing of a huge amount of digital data [4]. Digital signal processor (DSP) systems incorporate a multiplication unit to implement algorithms such as convolution and filtering. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of the algorithm. Multiplication is the most critical operation in every computational system [8]. Graphics and Process control are two more domains where in the multiplier performance plays a crucial role. The bottlenecks posed by multiplication in the above mentioned application areas are both temporal and spatial in nature. Therefore it appears that, custom VLSI implementations in the form of Application Specific Integrated Circuits (ASIC) or the DSP processors are the only viable alternatives to address the latency demands of such computationally intensive applications, that too without compromising the spatial aspects in view of the propagation delays [2]. However, even in the FPGA paradigm, the custom multiplication hardware embedded within a reconfigurable array has shown promising results and hence is a preferred choice currently due to the cost effective rapid prototyping design cycles as well as the possibility of concurrency, distributed
Accordingly, many researchers have implemented variants of the basic “Shift Addition” method to realize the multipliers in FPGA. Some of the preeminent methods of multiplier implementation in the FPGA paradigm are Scaling Accumulator, Ripple Carry Array, Carry Save Array, Look-Up Table and Partial Product, Computed Partial Product, and Wallace Trees. Amongst the above-mentioned multiplier implementations, the Wallace tree multipliers stimulate VLSI implementation interests reduce the depth of the adder chain thereby minimizing the time complexity.

The most efficient multiplier structure will vary depending on the throughput requirement of the application. The first step of the design process is the selection of the optimum circuit structure. There are various structures to perform the multiplication operation starting from the simple serial multipliers to the complex parallel multipliers [1]. Any speed improvement in the multiplier will improve the operating frequency of the digital signal processors or can be traded for energy by optimizing circuit sizes and the voltage supply.

This paper addresses high-level optimization techniques for Wallace Tree Multiplier multipliers. High-level techniques refer to algorithm and architecture level techniques that consider multiplication’s arithmetic features and input data characteristics. One of the important algorithm presents in paper for VLSI implementable multiplication is Wallace Tree Multiplier using Xilinx and Cadence tool.

II. PROPOSED METHOD

A fast process for multiplication of two numbers was developed by Wallace [7]. Using this method, a three step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product. In the Wallace Tree method, three bit signals are passed to a one bit full adder (“3W”) which is called a three input Wallace Tree circuit, and the output signal (sum signal) is supplied to the next stage full adder of the same bit, and the carry output signal thereof is passed to the next stage full adder of the same no of bit, and the carry output signal thereof is supplied to the next stage of the full adder located at a one bit higher position[5].

![Wallace Tree multiplier](image_url)
A 8-bit multiplier is constructed by using Wallace tree architecture. The architecture has been shown in Figure 3. Partial products are added in 6 steps. In the Wallace Tree method, the circuit layout is not easy although the speed of the operation is high since the circuit is quite irregular [3]. The delay generated in wallace tree multiplier can be further reduced by using modified tree structures called compressors.

### III. METHODOLOGY OF COMPRESSOR

Compressors are arithmetic components, similar in principle to parallel counters, but with two distinct differences: (1) they have explicit carry-in and carry-out bits; and (2) there may be some redundancy among the ranks of the sum and carry-output bits.

#### 1) 4:2 Compressor

The 4:2 compressor has 4 input bits and produces 2 sum output bits (out0 and out1), it also has a carry-in (cin) and a carry-out (cout) bit (thus, the total number of input/output bits are 5 and 3); All input bits, including cin, have rank 0; the two output bits have ranks 0 and 1 respectively, while cout has rank 1 as well. Thus, the output of the 4:2 compressor is a redundant number; for example, out1 = 0 and cout = 1 is equivalent to out1 = 1 and cout = 0 in all cases.

#### 2) 5:2 Compressor

The 5:2 compressor has 5 input bits and produces 2 sum output bits (sum and cout3), it also has a carry-in (cin1, cin2) and a carry-out (cout1, cout2, cout3) bit (thus, the total number of input/output bits are 7 and 4); All input bits, including cin1, have rank 0 and cin2 has rank 2; the two output bits have ranks 0 and 1 respectively, while cout2 has rank 1 and cout1 has rank 2 as shown in Fig
Fig. 4. 5:2 compressor I/O diagram.

Verification and simulation results:
Xilinx is powerful simulation tool for simulate and compile Verilog/VHDL code efficiently. All the basic modules designed for Wallace tree multiplier are compiled and tested vigorously for functional correctness using waveforms. The complete circuit of 16x16 bit Wallace tree multiplier is described in Verilog, as a structural component. The hieratical structure is created and the complete simulation can be observed.

IV. CONCLUSIONS
The Wallace tree multipliers can be solved & analyzed using a new modified method of Wallace tree construction using compressors. The modified tree has a slightly smaller critical path, a slightly larger wiring overhead but gives high speed.. This modified design of multiplier which consist of 7:2 compressor ,6:2 compressor ,5:2 compressor ,4:2 compressor, 3:2 compressor, full adders and reduced no. of half adder and reduces the complexity and reduce the time delay. Multiplier using Compressor have small increase in area and power but the time delay is less compare to conventional Wallace Tree Multiplier. As the Compressor order is increased the time delay reduces respectively. Hence for small delay requirement Wallace Tree Multiplier using compressor is suggested.

REFERENCES