DESIGN OF LOW POWER FLIP FLOP USING DUAL STACK METHOD FOR LOW LEAKAGE POWER

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Abstract: This paper enumerates low power, high speed design of flip-flop having less number of transistors and only one transistor being clocked by short pulse train which is true single phase clocking (TSPC) flip-flop. Compared to Conventional flip-flop, it has 5 Transistors and one transistor clocked, thus has lesser size and lesser power consumption. It can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The analysis for various flip flops and latches for power dissipation and propagation delays at 0.13μm and 0.35μm technologies is carried out. The leakage power increases as technology is scaled down. The leakage power is reduced by using best technique among all run time techniques viz. MTCMOS. Thereby comparison of different conventional flip-flops, latches and TSPC flip-flop in terms of power consumption, propagation delays and product of power dissipation and propagation delay with SPICE simulation results is presented.

I. INTRODUCTION

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. At each rising or falling edge of a clock signal, the data stored in a set of flip-flops is readily available so that it can be applied as inputs to other Combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered flip-flops otherwise it is called as single edge triggered flip-flops. When technology scales down, total power dissipation will decrease and at the same time delay varies depends upon supply voltage, threshold voltage, aspect ratio, oxide Thickness, load capacitance. CMOS devices have scaled downward aggressively in each technology generation to achieve higher integration density and performance. However leakage current has increased drastically with technology scaling and become a major contributor to the total IC power.

II. BRIEF LITERATURE REVIEW

A. 8 Transistor T flip-flop and 6 transistor latch circuit

8 Transistors flip-flop the pioneer CMOS traditional flipflop circuit is reported. 6 transistor latch is built using 4 NMOS and 2 PMOS transistors

B. 5 Transistors proposed TSPC flip-flop

The schematic of proposed TSPC flip-flop is shown in Fig. 1. This flip-flop is built using 4 NMOS and 2 PMOS transistors

Keywords: CMOS, figure of merit, leakage current, power, delay, TSPC flip-flop
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Fig. 1 shows positive edge triggered 5 Transistor D latch. When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the values of input it becomes output. It also acts as a flip-flop when the input IN has less pulse width.

IV. LEAKAGE POWER ANALYSIS

Minimization power consumption is essential for high performance VLSI systems. In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation. Furthermore, the leakage power also becomes highly significant. High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced [6-8]. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power especially for low-power applications. Multivariable Threshold voltage CMOS (MTCMOS) and voltage scaling are two of the methods to reduce power.

V. MTCMOS TECHNIQUE

MTCMOS is one of the important low power techniques and is used to reduce the leakage. Fig. 2 shows TSPC FF with this technique.

To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal mode.

VI. NOVEL DUAL STACK APPROACH

In this section, the structure and operation of our novel low-leakage-power design is described. Here we use 2 pmos in the pull-down network and 2 nmos in the pullup network. The advantage is that nmos degrades the high logic level while pmos degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit. As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention.
VII. SIMULATION METHODOLOGY

To show that the dual stack approach is applicable to general logic and memory design, we choose a FLIP FLOP and a SRAM cell. We use Avant! Star-HSPICE to estimate delay and power consumption. Area is estimated with the help of MICROWIND. The FLIP FLOP each with W/L=6 for PMOS and W/L=3 for NMOS for the base case. Sleep transistors in the sleep approach (Fig. 1) are sized such that any sleep transistor between VDD and a pull-up network takes the size of the largest transistor in the pull-up network, and any sleep transistor between GND and a pull-down network takes the size of the largest transistor in the pull-down network. For example, sleep transistors used in the pull-up and pull-down networks of the base case inverter chain have W/L=6 and W/L=3. Transistors in the stack approach are sized to half of the size of the base case transistors, e.g., transistors used in pull-up and pull-down of the base case inverter chain have W/L=3 and W/L=1.5, respectively. Similarly, transistors, including sleep transistors, in the sleepy stack approach are sized to half of the size of the base case transistors.
IX. CONCLUSION

In nanometer scale CMOS technology, subthreshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named “Dual stack” as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product.

REFERENCES

9. TSPICE: http://www.tanner.com